Fig.1

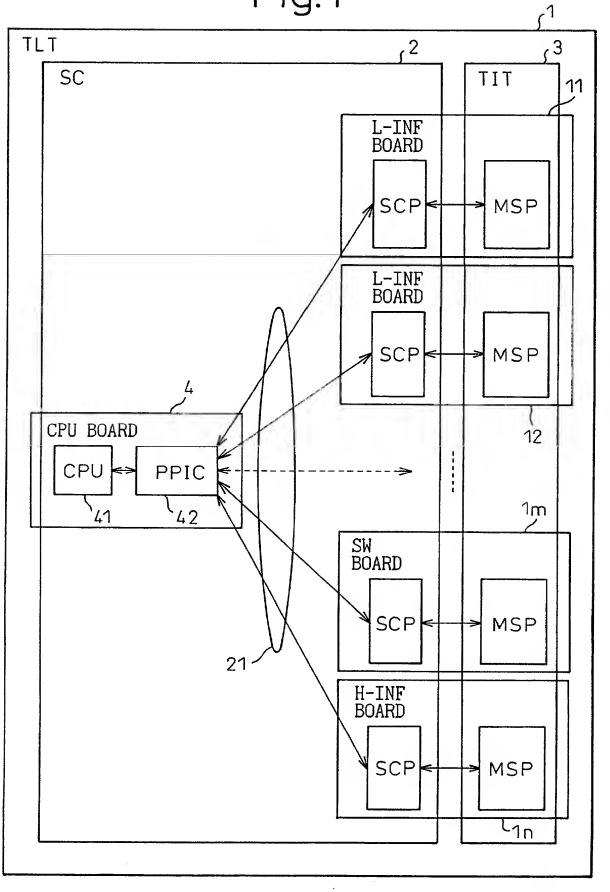

1
TLT
2
SC
3
TIT
11
L-INF BOARD
SCP
MSP
L-INF BOARD
SCP
MSP
12
4
CPU BOARD
CPU
PPIC
41
42
1m
SW BOARD
SCP
MSP
21
H-INF BOARD
SCP
MSP
1n

Fig.2

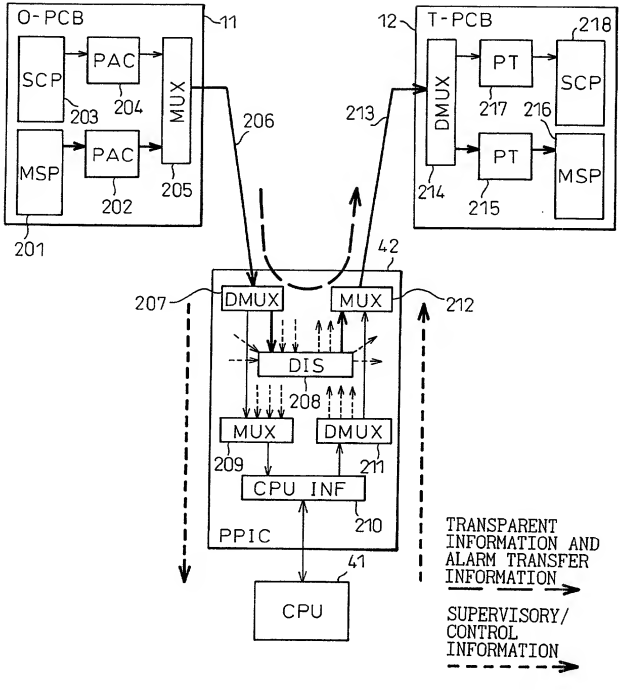

O-PCB
11
SCP
PAC
203
204
MUX
MSP
PAC
202
205
201
206
12
T-PCB
218
DMUX
PT
SCP
217
216
213
PT
MSP
214
215
42
207
DMUX
MUX
212
DIS
208
MUX
DMUX
209
211
CPU INF
210
PPIC
41
CPU
TRANSPARENT INFORMATION AND ALARM TRANSFER INFORMATION
SUPERVISORY/ CONTROL INFORMATION

Fig.3A

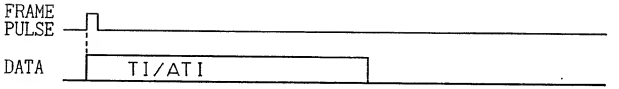


Fig.3B

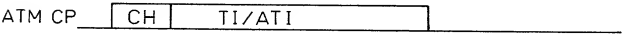
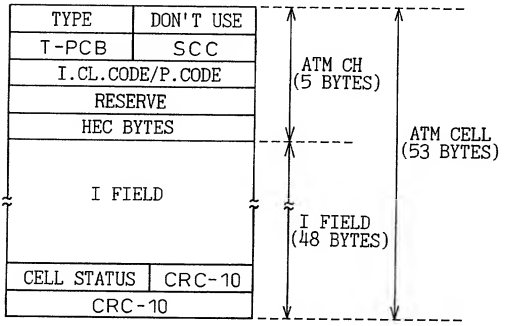


Fig.3C



2052207 "2526804

Fig.3D

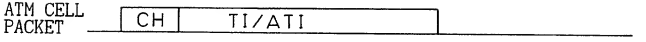


Fig.3E

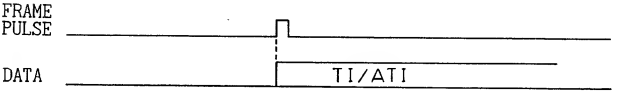


Fig.4

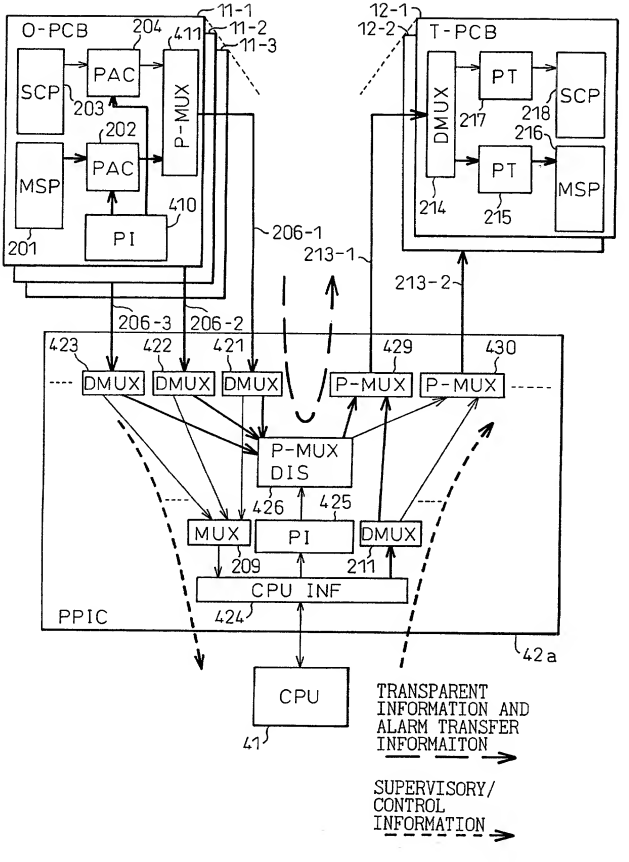

O-PCB
T-PCB
SCP
MSP
PAC
PAC
P-MUX
PI
DMUX
PT
PT
SCP
MSP
11-1
11-2
11-3
12-1
12-2
201
202
203
204
410
411
214
215
216
217
218
206-1
206-2
206-3
213-1
213-2
423
422
421
429
430
DMUX
DMUX
DMUX
P-MUX
P-MUX
P-MUX DIS
426
425
MUX
PI
DMUX
209
211
CPU INF
424
PPIC
42a
CPU
41
TRANSPARENT INFORMATION AND ALARM TRANSFER INFORMAITON
SUPERVISORY/ CONTROL INFORMATION

Fig.5

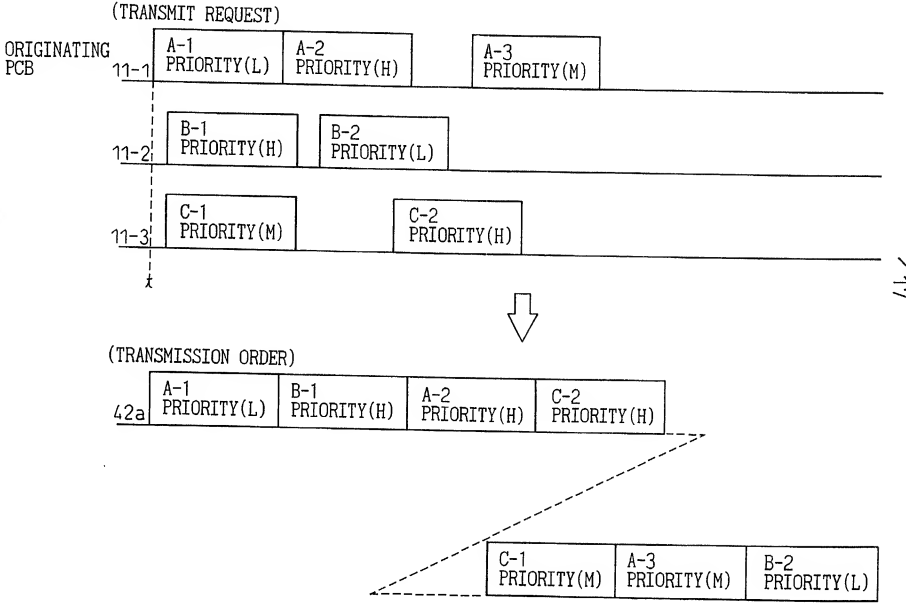

(TRANSMIT REQUEST)
ORIGINATING PCB
11-1
A-1 PRIORITY(L)
A-2 PRIORITY(H)
A-3 PRIORITY(M)
11-2
B-1 PRIORITY(H)
B-2 PRIORITY(L)
11-3
C-1 PRIORITY(M)
C-2 PRIORITY(H)
t
(TRANSMISSION ORDER)
42a
A-1 PRIORITY(L)
B-1 PRIORITY(H)
A-2 PRIORITY(H)
C-2 PRIORITY(H)
C-1 PRIORITY(M)
A-3 PRIORITY(M)
B-2 PRIORITY(L)

Fig.6

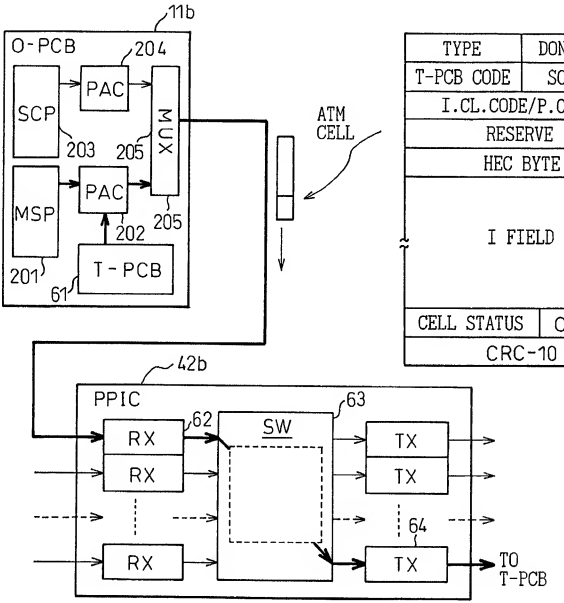

11b
O-PCB
204
PAC
SCP
203
205
MUX
PAC
MSP
202
205
201
T-PCB
61
ATM CELL
TYPE
DON'T USE
T-PCB CODE
SC CODE
I.CL.CODE/P.CODE
RESERVE
HEC BYTE
I FIELD
CELL STATUS
CRC-10
CRC-10
42b
PPIC
63
62
SW
RX
RX
RX
TX
TX
TX
64
TO
T-PCB

Fig.7

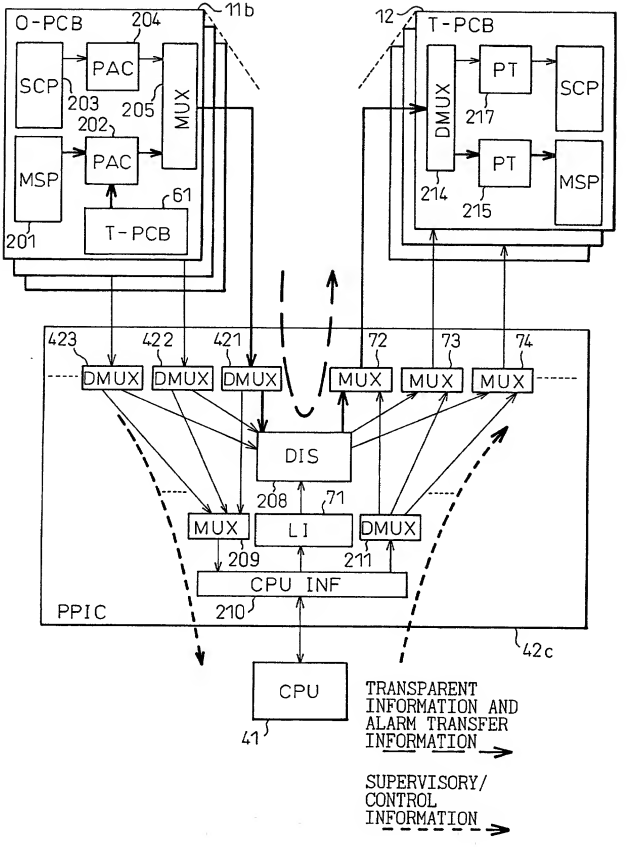

O-PCB
204
11b
SCP
PAC
203
205
MUX
202
MSP
PAC
61
201
T-PCB
12
T-PCB
DMUX
PT
SCP
217
PT
MSP
214
215
423
422
421
72
73
74
DMUX
DMUX
DMUX
MUX
MUX
MUX
DIS
208
71
MUX
LI
DMUX
209
211
CPU INF
210
PPIC
42c
CPU
41
TRANSPARENT INFORMATION AND ALARM TRANSFER INFORMATION
SUPERVISORY/ CONTROL INFORMATION

Fig.8

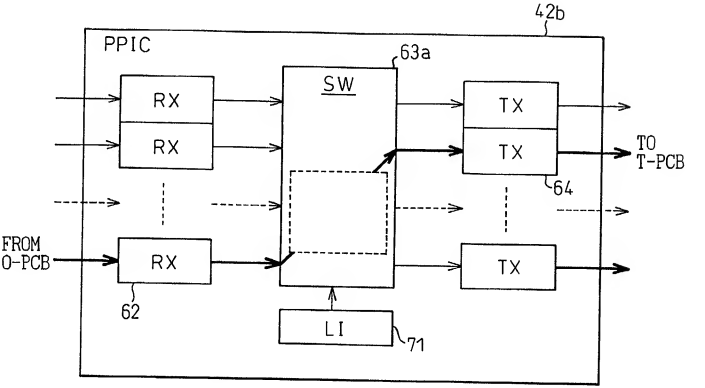


Fig.9

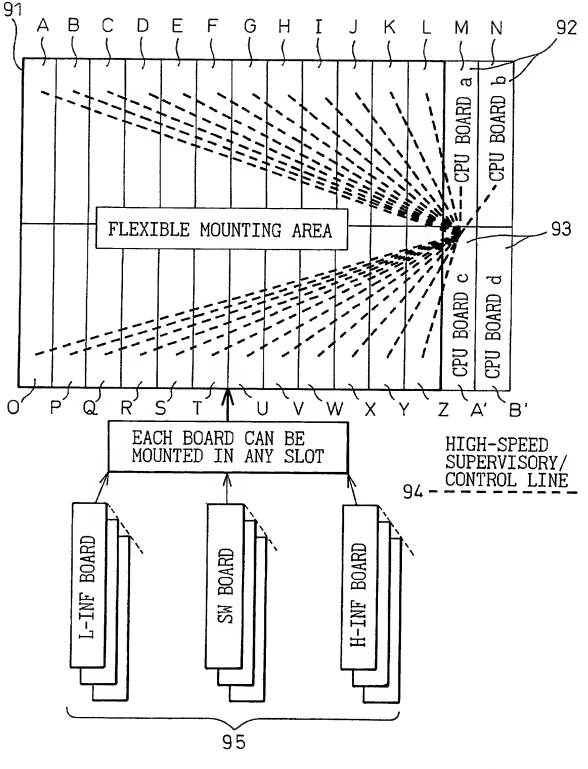


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Fig.10

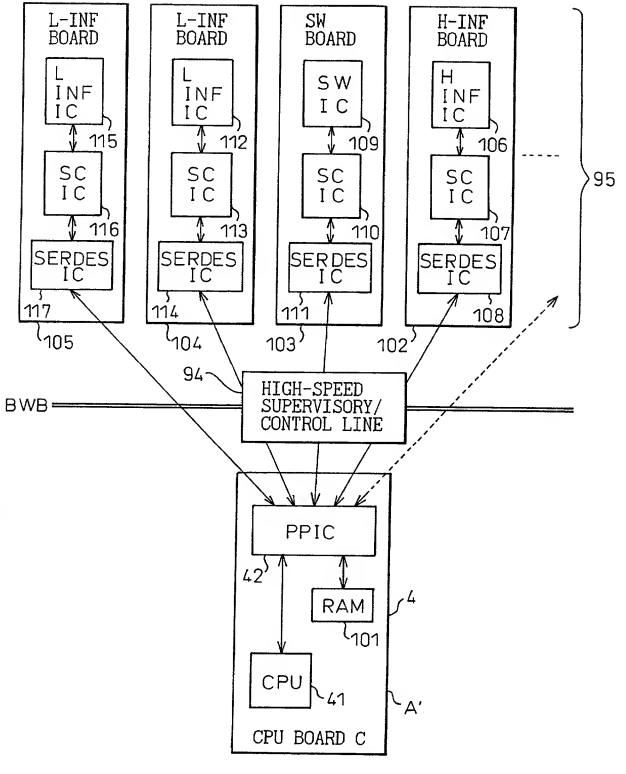

L-INF BOARD
L INF IC
115
SC IC
116
SERDES IC
117
105
L-INF BOARD
L INF IC
112
SC IC
113
SERDES IC
114
104
SW BOARD
SW IC
109
SC IC
110
SERDES IC
111
103
H-INF BOARD
H INF IC
106
SC IC
107
SERDES IC
108
102
95
94
HIGH-SPEED SUPERVISORY/ CONTROL LINE
BWB
PPIC
42
RAM
101
4
CPU
41
A'
CPU BOARD C

Fig.11

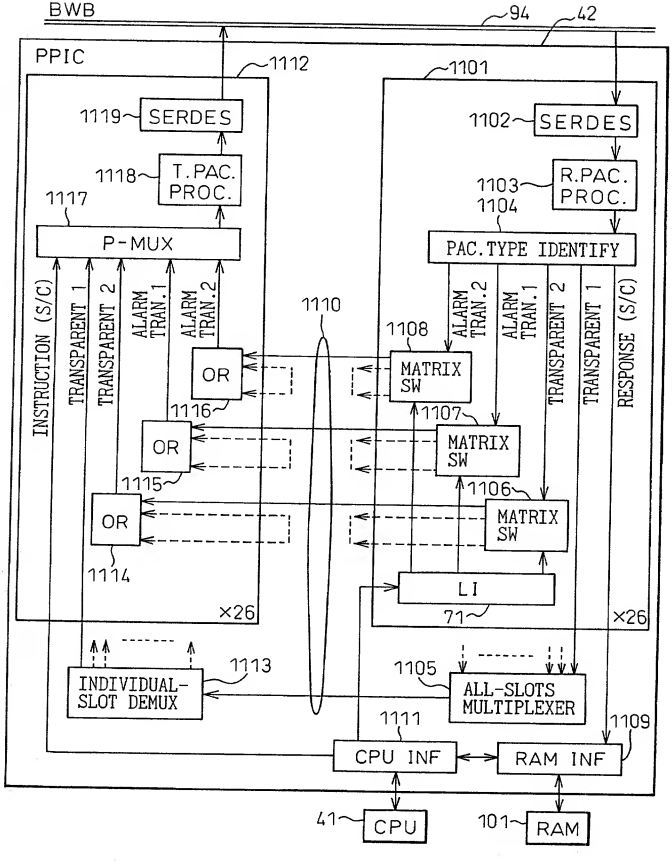

BWB
94
42
PPIC
1112
1101
1119
SERDES
1102
SERDES
1118
T.PAC. PROC.
1103
1104
R.PAC. PROC.
1117
P-MUX
PAC.TYPE IDENTIFY
INSTRUCTION (S/C)
TRANSPARENT 1
TRANSPARENT 2
ALARM TRAN.1
ALARM TRAN.2
1110
1108
ALARM TRAN.2
ALARM TRAN.1
TRANSPARENT 2
TRANSPARENT 1
RESPONSE (S/C)
OR
MATRIX SW
1116
1107
OR
MATRIX SW
1115
1106
OR
MATRIX SW
1114
LI
71
×26
×26
1113
INDIVIDUAL-SLOT DEMUX
1105
ALL-SLOTS MULTIPLEXER
1111
1109
CPU INF
RAM INF
41
CPU
101
RAM

Fig.12

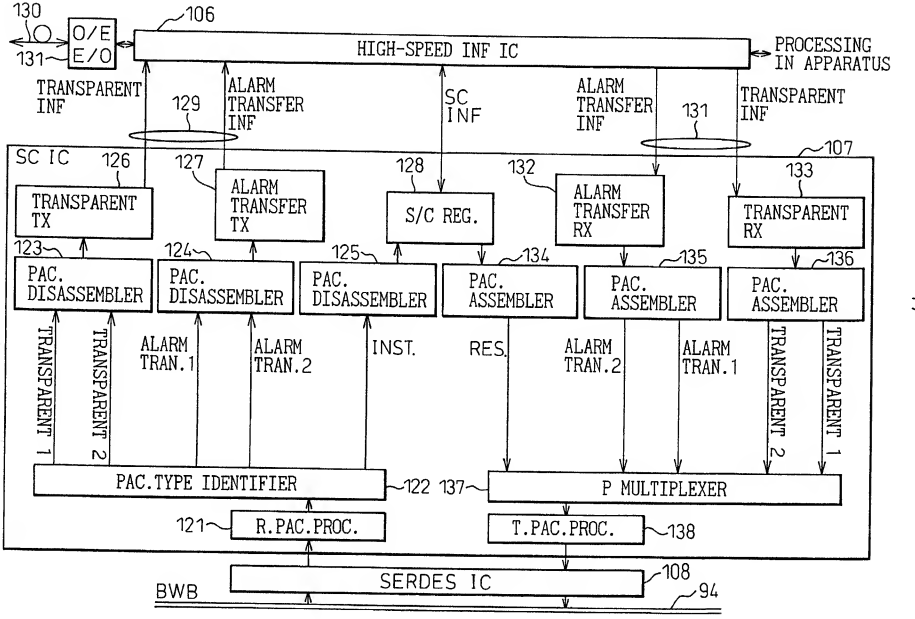
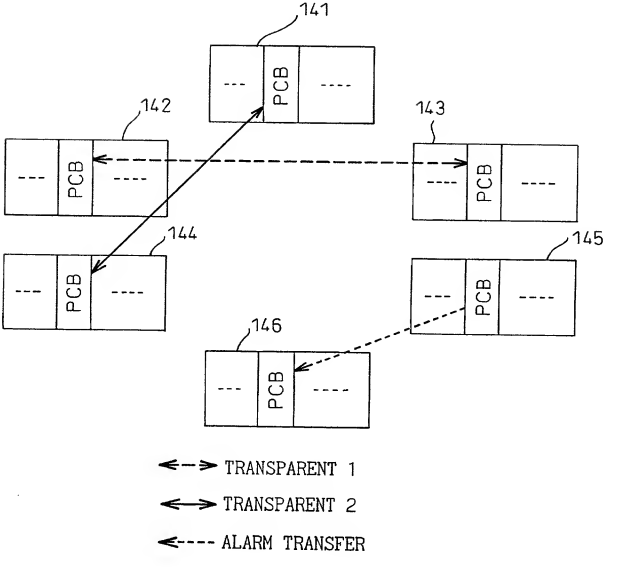

130
O/E
E/O
131
106
HIGH-SPEED INF IC
PROCESSING IN APPARATUS
TRANSPARENT INF
129
ALARM TRANSFER INF
SC INF
ALARM TRANSFER INF
131
TRANSPARENT INF
SC IC
126
127
128
132
133
107
TRANSPARENT TX
ALARM TRANSFER TX
S/C REG.
ALARM TRANSFER RX
TRANSPARENT RX
123
124
125
134
135
136
PAC. DISASSEMBLER
PAC. DISASSEMBLER
PAC. DISASSEMBLER
PAC. ASSEMBLER
PAC. ASSEMBLER
PAC. ASSEMBLER
TRANSPARENT 1
TRANSPARENT 2
ALARM TRAN.1
ALARM TRAN.2
INST.
RES.
ALARM TRAN.2
ALARM TRAN.1
TRANSPARENT 2
TRANSPARENT 1
PAC.TYPE IDENTIFIER
122
137
P MULTIPLEXER
121
R.PAC.PROC.
T.PAC.PROC.
138
108
SERDES IC
BWB
94

Fig.13



EP 0 952 707 A2 20021009

Fig.14

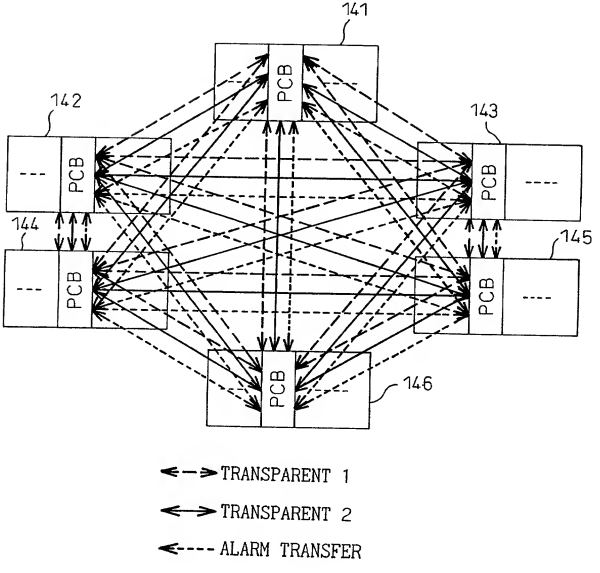

141
142
143
144
145
146
PCB
TRANSPARENT 1
TRANSPARENT 2
ALARM TRANSFER

Fig.15

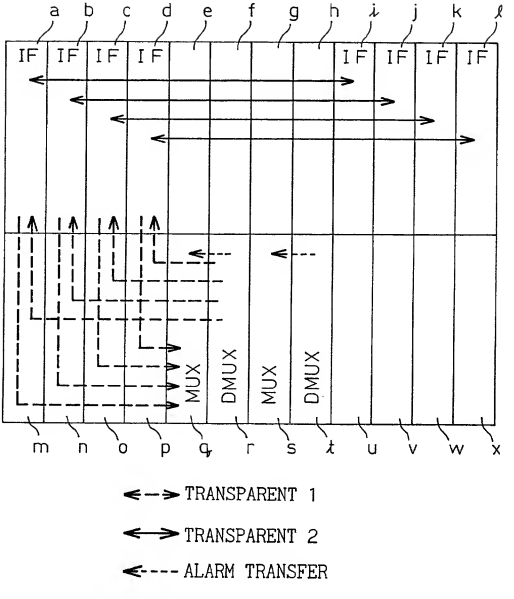
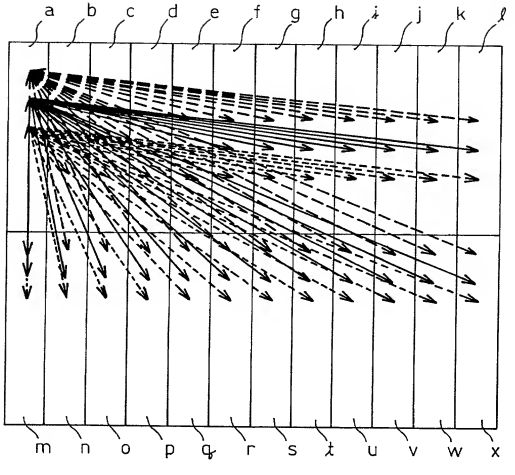

a
b
c
d
e
f
g
h
i
j
k
l
IF
IF
IF
IF
IF
IF
IF
IF
MUX
DMUX
MUX
DMUX
m
n
o
p
q
r
s
t
u
v
w
x
TRANSPARENT 1
TRANSPARENT 2
ALARM TRANSFER

Fig.16


a
b
c
d
e
f
g
h
i
j
k
l
m
n
o
p
q
r
s
t
u
v
w
x
TRANSPARENT 1
TRANSPARENT 2
ALARM TRANSFER